CHAPTER 09 QUESTIONS

MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question.

1) When setting the voltage for an external device that must interface with an FPGA, you must change the value of ________.
   A) $V_{CCIO}$    B) $V_{DDIN}$    C) $V_{DDIO}$    D) $V_{CCIN}$

2) Which of the following digital IC logic families is most susceptible to static discharge?
   A) RTL     B) ECL     C) MOS     D) TTL

3) Which of the following is a concern when using CMOS type devices?
   A) mechanical shock  B) electrostatic discharge  C) fan out  D) under voltage

4) Which of the following is not a solution to interface problems between CMOS and TTL?
   A) pull-up resistor  B) pull-down resistor  C) level-shifter  D) buffer

5) Which of the following is not a common logic family used today?
   A) RTL     B) ECL     C) TTL     D) CMOS

6) The output current for a LOW output is called a(n)
   A) exit current.  B) sink current.  C) ground current.  D) fan-out.

7) Which of the following are not characteristics of TTL logic gates?
   A) Totem-pole output  B) Bipolar transistors  C) CMOS transistors  D) Multiemitter transistors

8) Which of the following output levels would not be a valid LOW for a TTL gate?
   A) 0.3 V  B) 0.5 V  C) 0.2 V  D) All are valid.

9) A family of logic devices designed for extremely high speed applications is called
   A) NMOS.  B) ECL.  C) PMOS.  D) TTL.

10) Unused inputs on TTL, AND, and NAND gates
    A) degrade the gate’s noise immunity.  B) if left open will have the same effect as HIGH inputs.  C) should be tied HIGH.  D) All of the above are correct.

11) The lower transistor of a totem-pole output is OFF when the gate output is
    A) HIGH.  B) malfunctioning.  C) LOW.  D) over driven.

12) The input transistor on a TTL circuit is unusual in that it has
    A) multiple bases.  B) no collector.  C) no base.  D) multiple emitters.
13) The 54XX TTL IC series is the military version and has
A) a wider temperature range.
B) more stringent power supply requirements.
C) higher current output capability.
D) all of the above.

14) Which potential problem must be overcome when interfacing TTL to CMOS?
A) The HIGH output voltage may be too low.
B) The LOW output voltage may be too high.
C) The HIGH output voltage may be too high.
D) The output current may not be sufficient.

15) Typical TTL LOW level output voltage is
A) 0.3 V.  B) 0.0 V.  C) 3.4 V.  D) 4.0 V.

16) When the outputs of several open-collector TTL gates are connected together, the gate outputs
A) produce more fan-out.  B) usually burn out.  C) are ANDed together.  D) produce more voltage.

17) The abbreviated designation for output current with a LOW output is
A) IOL.  B) IOH.  C) IOH.  D) IIL.

18) The input transistor (Q 1) of a TTL gate acts like
A) a NAND gate.  B) a NOR gate.  C) an AND gate.  D) an OR gate.

19) The unused input for a NOR gate should be tied to
A) HIGH.  B) ground.  C) another unused input.  D) both B and C

20) Which of the following output levels would be a valid HIGH for a TTL gate?
A) 3.0 V  B) 2.6 V  C) 5.1 V  D) All are valid.

21) The noise margin for a standard TTL gate is
A) 1.0 V.  B) 0.4 V.  C) 1.4 V.  D) 0.8 V.

22) When a TTL gate output connects to a CMOS gate, what must be added to the circuit?
A) a decoupling capacitor  B) a pull-up resistor  C) a pull-down resistor  D) an open-collector gate

23) Which of the following levels would not be a valid LOW for a TTL gate?
A) 0.1 V  B) 0.7 V  C) 1.0 V  D) All are valid.

24) What advantage does the 74HXX series device have over standard TTL?
A) reduced propagation delay  B) higher propagation delay  C) low power consumption  D) lower voltage requirements

25) The CMOS series that is pin compatible with the TTL family is the
A) 74C00 series.  B) 4000 series.  C) 5400 series.  D) 7400 series.
26) The propagation delay of standard TTL gates is approximately
   A) 2 µsec.       B) 10 nsec.       C) 4 nsec.       D) 1 µsec.

27) Which alteration is made in the manufacture of a TTL gate to create an open-collector output?
   A) The output transistors are replaced by diodes.
   B) The input transistor is replaced by a diode.
   C) The output transistors are missing.
   D) The top output transistor is missing.

28) One advantage that MOSFET transistors have over bipolar transistors is
   A) reduced propagation delay.
   B) higher switching speed.
   C) high input impedance.
   D) low input impedance.

29) The original CMOS line of circuits is the
   A) 5400 series.       B) 4000 series.
   C) 74C00 series.       D) 74HCOO series.

30) When a CMOS gate output connects to a TTL gate, which circuit is needed?
   A) a decoupling capacitor
   B) a pull-up resistor
   C) a pull-down resistor
   D) a CMOS buffer

31) The abbreviated designation for output current with a HIGH output is
   A) IOH.       B) IIL.       C) I IH.       D) IOL.

32) The abbreviated designator for a HIGH input voltage is
   A) VOH.       B) VIH.       C) VIL.       D) VOL.

33) A common means for comparing the propagation delays and the power dissipation of various logic gates is the
   A) fan-out.
   B) power requirements.
   C) speed-power product.
   D) noise margin.

34) When interfacing CMOS to TTL what potential problem must be overcome?
   A) There may be insufficient current.
   B) The low output voltage may be insufficient.
   C) The output current may be too great.
   D) The high voltage may be too low.

35) The abbreviated designator for a HIGH output voltage is
   A) VIL.       B) VOH.       C) VIH.       D) VOL.

36) The difference between VOH and VIH voltages is known as
   A) input margin.
   B) noise margin.
   C) output differential.
   D) input level.

37) The maximum output voltage recognized as a LOW by a TTL gate is
   A) 2.0 V.       B) 0.8 V.       C) 2.4 V.       D) 0.4 V.
38) The primary advantage of ECL over TTL is that ECL integrated circuits have
A) very low power dissipation.   B) low noise margins.
C) very short propagation delay times.   D) both A and C

39) The output current capability for a HIGH output condition is called a(n)
A) source current.   B) exit current.   C) sink current.   D) fan-out.

40) The upper transistor of a totem-pole output is saturated when the gate output is
A) shorted.   B) HIGH.   C) logic 0.   D) LOW.

41) The time it takes for a square wave to go from 10% to 90% of its voltage level is called
A) fan-out.   B) rise time.   C) propagation delay.   D) fall time.

42) The number of gates that can be connected to a single output without exceeding the current ratings of the gate is called
A) dissipation.   B) propagation.   C) fan-out.   D) SSI.

43) Which of the following input levels would not be a valid HIGH for a TTL gate?
A) 2.4 V   B) 2.1 V   C) 1.8 V   D) All are valid.

44) Each input on a TTL gate is connected to the transistor’s

45) The time it takes for an input signal to pass through internal circuitry and generate the appropriate output effect is known as
A) propagation delay.   B) rise time.   C) fan-out.   D) fall time.

46) The maximum input voltage recognized as a LOW by a TTL gate is
A) 2.4 V.   B) 0.8 V.   C) 0.0 V.   D) 0.4 V.

47) The abbreviated designation for input current with a HIGH input is
A) \(V_{IH}\).   B) \(I_{IH}\).   C) \(I_{IL}\).   D) \(I_{OL}\).

48) The output stage of a TTL gate is a special design called a(n)
A) totem-pole.   B) DIP.   C) MSI.   D) multiemitter.

49) Which specialized device distinguishes the 74LSXX circuits from standard 74XX circuits?
A) a Schottky diode   B) a CMOS transistor
C) a multiemitter transistor   D) totem-pole output transistor

50) An open-collector TTL gate
A) must have an external pull-up resistor to produce a LOW.
B) must have an external pull-up resistor to produce a HIGH.
C) must have an external ground connected to the output to produce a LOW.
D) must have a transistor added to the output to produce a HIGH.
51) The abbreviated designator for a LOW input voltage is
   A) \( V_{IL} \)  \quad \text{B) } V_{OH} \quad \text{C) } V_{OL} \quad \text{D) } V_{IH}.

52) What advantage does the 74LXX series device have over standard TTL?
   A) lower voltage requirements  \quad \text{B) } reduced propagation delay
   C) higher propagation delay  \quad \text{D) } low power consumption

53) When the outputs of several standard TTL gates are connected together, the gate outputs
   A) enable new logic configurations.  \quad \text{B) } produce more fan-out.
   C) usually burn out.  \quad \text{D) } produce more voltage.

54) Which of the following is a special type of transistor used in the TTL series to improve speed
   characteristics?
   A) Belrus  \quad \text{B) } Shockley  \quad \text{C) } Brattain  \quad \text{D) } Schottky

55) The upper transistor of a totem-pole output is OFF when the gate output is
   A) logic 1.  \quad \text{B) } malfunctioning.
   C) HIGH.  \quad \text{D) } LOW.

56) The major advantage of TTL logic circuits over CMOS is
   A) lower propagation delay.  \quad \text{B) } the ability to output higher voltages.
   C) more modern design.  \quad \text{D) } very low power consumption.

57) The maximum current for a HIGH output on a standard TTL gate is
   A) -10 \( \mu \)A.  \quad \text{B) } -400 \( \mu \)A.  \quad \text{C) } -1 \( \mu \)A.  \quad \text{D) } -10 mA.

58) The maximum current for a LOW output on a standard TTL gate is
   A) 16 \( \mu \)A.  \quad \text{B) } 40 mA.  \quad \text{C) } 100 \( \mu \)A.  \quad \text{D) } 16 mA.

59) The major advantage of CMOS logic circuits over TTL is
   A) very low power consumption.
   B) the ability to produce several output voltage levels.
   C) lower propagation delay.
   D) much higher propagation delay.

60) The abbreviated designation for input current with a LOW input is
   A) \( I_{IH} \)  \quad \text{B) } I_{IL} \quad \text{C) } I_{OL} \quad \text{D) } I_{OL}.

61) The time it takes for a square wave to go from 90\% to 10\% of its voltage level is called
   A) rise time.  \quad \text{B) } fan-out.
   C) fall time.  \quad \text{D) } propagation delay.

62) What advantage does the 74SXX series device have over standard TTL?
   A) higher propagation delay  \quad \text{B) } lower voltage requirements
   C) low power consumption  \quad \text{D) } reduced propagation delay
63) What advantage does the 74LSXX series device have over standard TTL?  
   A) higher propagation delay  
   B) reduced propagation delay  
   C) low power consumption  
   D) low power consumption and reduced propagation delay  

64) An invalid input voltage for a TTL logic gate would be  
   A) less than 0.8 V.  
   B) greater than 2.0 V but less than 5.0 V.  
   C) greater than 2.0 V.  
   D) between 0.8 V and 2.0 V.  

65) Fan-out for a typical TTL gate is ________.
   A) 10  
   B) 4  
   C) 54  
   D) 100  

66) In order to interface an FPGA with an external device, you must set the value of the  
   A) sink current.  
   B) external power supply.  
   C) source current.  
   D) all of the above  

67) The abbreviated designator for a LOW output voltage is  
   A) V_{OH}.  
   B) V_{IL}.  
   C) V_{OL}.  
   D) V_{IH}.  

68) The lower transistor of a totem-pole output is saturated when the gate output is  
   A) HIGH.  
   B) LOW.  
   C) malfunctioning.  
   D) over driven.  

69) The abbreviation TTL means  
   A) transistor-transceiver latch.  
   B) three-transistor logic.  
   C) two-transistor logic.  
   D) transistor-transistor logic.  

70) Typical TTL HIGH level output voltage is  
   A) 0.3 V.  
   B) 5.0 V.  
   C) 3.4 V.  
   D) 4.8 V.  

71) The standard 74XX TTL IC family was originally developed in the  
   A) 1970s.  
   B) 1960s.  
   C) 1950s.  
   D) 1940s.  

72) The minimum output voltage recognized as a HIGH by a TTL gate is  
   A) 0.8 V.  
   B) 2.4 V.  
   C) 5.0 V.  
   D) 2.0 V.  

73) An open-collector TTL gate  
   A) can sink current but cannot source current.  
   B) can source current but cannot sink current.  
   C) cannot source or sink current.  
   D) can sink more current than a standard TTL gate.  

74) The minimum input voltage recognized as a HIGH by a TTL gate is  
   A) 0.8 V.  
   B) 2.4 V.  
   C) 2.0 V.  
   D) 5.0 V.
Answer Key
Testname: CHAP09Q

1) A
2) C
3) B
4) B
5) A
6) B
7) C
8) D
9) B
10) D
11) A
12) D
13) A
14) A
15) A
16) C
17) B
18) C
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